Design Concepts for High-Power *PIN* Diode Limiting

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Abstract—**Experimental data and discussion are presented which show the desirability of using thick punch-through *PIN* diode for high-power limiting. The slower speed of response sets an upper limit on thickness. Data are presented on the maximum thickness allowable as a function of frequency. Results are given for a high-peak-power narrow-pulsewidth receiver protector, and for a high-average-power wide-pulsewidth balanced duplexer. These devices are compared to conventional gas T–R tubes and results suggest that the use of multiple *PIN* diodes in limiters and duplexers can offer significant improvements in some radar applications.**

Introduction

THE USE OF semiconductor diodes for limiting and switching microwave power has been widely discussed by various authors over the last ten years.[1]–[6] In spite of this, the technique of high-power limiting in the megawatt peak power region has not been achieved. One reason, undoubtedly, has been the lack of suitable diodes. The varactor diode is used as a high-power limiter up to the tens of kilowatts peak power; however, it is impractical to use this diode in high-power applications because of its small junction size. Junction size is the determining factor in the ability of diodes to handle large amounts of power.

The high-voltage *PIN* diode has excellent power handling properties. However, this diode has a thick *I* (intrinsic) region, and consequently, its speed of response is far too slow to allow its use as a self-switching device. One technique that has circumvented this "turn on" problem with the *PIN* diode is the use of a point-contact rectifier diode (crystal) to provide the biasing current.[7] Generally, this is accomplished by inserting a coupling loop into the line to pick up rectified crystal current sufficient to drive the *PIN* into conduction. The disadvantage of this technique is that a finite turn-on time exists on the order of 100 ns, which allows the passage of a large spike leakage. In many cases, this spike leakage can be eliminated by a second stage using varactor diodes. Since the second stage is decoupled by the *PIN* diode stage over most of the pulsewidth, power handling is not a problem. A serious problem, however, is the complexity involved in installing and adjusting many bias crystals when a large number of *PIN* diodes are required.

The availability of a diode similar to the *PIN*, but without its attendant turn-on problem, would offer a substantial simplification in limiter design. There is such a diode available, designated a thin-base *PIN*, which will be examined in more detail later.

Manuscript received June 5, 1967; revised August 21, 1967.

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Although the basic purpose of this paper is to describe a high-power limiter using these thin-base *PIN* diodes, a wider scope is presented in order to emphasize the advantages of large junction diode devices and to examine the logic leading to the development of such a diode. Once evaluated, a number of interesting comparisons are made to the more conventional varactor and *PIN* diode devices and to another technology altogether, i.e., the gas discharge T–R tube. Two examples of devices using the thin-base *PIN* diode are discussed; the first is a high-peak-power narrow-pulsewidth receiver protector limiter, and the second, a medium-peak-power wide-pulsewidth all-diode duplexer.

Diode Limiter Circuit Constraints

The basic function of a high-power limiter is receiver protection; therefore, it must be a highly reflective device upon the application of high power. For system simplicity, the limiter should be self actuating, thus avoiding the complexities of programmed biasing. To handle maximum power, the limiter should have a low absorption loss. Good thermal properties are necessary to minimize heating effects caused by power absorption within the junction. A number of possible circuit configurations are presented in Fig. 1. These circuits will be discussed after the diode performance has been calculated for both series and shunt diode mounting configurations.

Since the topic of this paper is high-power diode limiting in the UHF range, a low-frequency model of the diode equivalent circuit will be used. Fig. 2(a) indicates the diode equivalent circuit, with L representing the diode inductance, C_J the junction capacity, R_s the series (small signal) resistance, R_F the conduction (large signal) series resistance, and C_p the diode package capacitance.

For small signals, the switch is considered open and the circuit can be reduced to Fig. 2(b). The parasitic reactances associated with L and C_p can be neglected in the UHF range. The value of C_J typically ranges from 0.5 to 5.0 pF. In order to parallel resonate this capacitance for minimum reflection loss, a shunt inductor L_p is often employed. A parallel equivalent circuit is also shown in Fig. 2(b) since it is useful for insertion loss calculations. The parallel resistor R_p is a function of the diode Q.

For high-power signals requiring limiting, the switch shown in Fig. 2(a) is considered closed and the circuit can be reduced to Fig. 2(c). The rather large reactance associated with the package capacity C_p can be ignored at UHF, but, unfortunately, the series inductance L cannot. This inductance can be series resonated with a bypass capacitor, but this has the disadvantage of returning the diode to ground

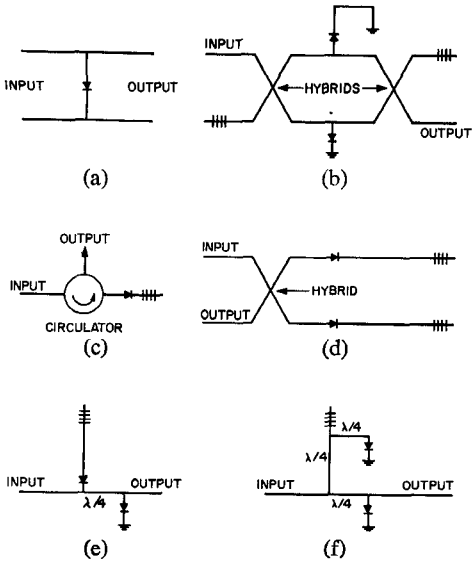


Fig. 1. Various limiter circuit configurations. (a) Shunt diode limiter. (b) Balanced shunt diode limiter. (c) Series diode limiter. (d) Balanced series diode limiter. (e) Branched limiter. (f) Branched limiter.

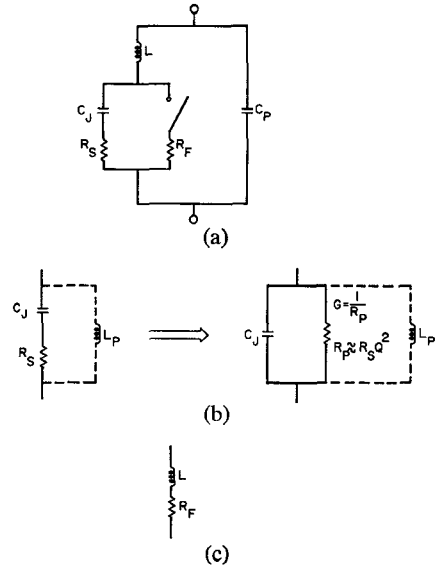


Fig. 2. *PIN* diode equivalent circuit. (a) Diode equivalent circuit. (b) Low-level receive state. (c) High-power conducting state.

through a dielectric, thus reducing the effectiveness of the heat removal path.

Examining the low-level receive state, a few definitions are necessary. The Q of a lossy capacitor (diode) is given by

$$Q_D = \frac{1}{\omega C_J R_s} \cdot \tag{1}$$

By definition, the cutoff frequency for the diode is

$$f_{co} = \frac{1}{2\pi C_J R_s} \cdot \tag{2}$$

Therefore the diode Q is given by

$$Q_D = \frac{f_{co}}{f_0} \cdot \tag{3}$$

Low-Power Loss

Shunt Mounted Diode–Transmission Limiter

The insertion loss α of a shunt mounted diode is

$$\alpha_{SH} = 10 \log \left[\left(1 + \frac{1}{2} \frac{G}{Y_0}\right)^2 + \left(\frac{1}{2} \frac{B}{Y_0}\right)^2 \right] \quad \text{(dB)}. \tag{4}$$

Assuming the susceptance is zero by the effects of parallel tuning with L_p, and that the shunt conductance G is considerably less than the line admittance the loss becomes

$$\alpha_{SH} \approx 10 \log \left[1 + \frac{G}{Y_0}\right] = 10 \log \left[1 + \frac{Z_0}{R_p}\right]. \tag{5}$$

For small values of loss

$$\alpha_{SH} \approx 4.34 \frac{Z_0}{R_p} \quad \text{(dB)}. \tag{6}$$

In terms of fractional power loss the insertion loss is

$$\alpha_{SH} \approx \frac{Z_0}{R_p} \cdot \tag{7}$$

Using the parallel equivalent circuit of Fig. 2(b), the insertion loss can be expressed in terms of the diode Q

$$\alpha_{SH} \approx \frac{Z_0}{R_s Q^2} \approx Z_0 \omega^2 C_J^2 R_s. \tag{8}$$

Series Mounted Diode–Reflection Limiter

In the series-mounted diode small signal state, the diode essentially terminates in an open-circuited transmission line causing the line voltage to double across the diode and raising the insertion loss by a factor of four.

$$\alpha_{SE} \approx 4 \frac{Z_0}{R_p} \cdot \tag{9}$$

This insertion loss for the series diode is the result of its reflection properties. Subsequent expressions for high-power isolation and loaded Q characteristics will also be based on the reflection properties of the series diode. Low insertion loss results from a highly reflecting diode, whereas, high isolation is the result of a low-reflection (conductive) diode.

High-Power Loss

Under high-power conditions the diode junction capacity is essentially shorted out and the circuit is as shown in Fig. 2(c). When direct (rectified) current flows, the conducting resistance R_F may be significantly less than the diode series resistances R_s because of the increase in density of charge carriers in the semiconductor due to the effects of conductivity modulation. To include the effects of conductivity

modulation, the diode forward resistance is designated R_F, and is less than R_s. In this state the power absorbed P_{DSH} becomes

$$P_{DSH} = P_L \frac{4R_F}{Z_0} \tag{10}$$

where P_L is the incident line power. The power absorbed P_{DSE} within a series-mounted diode becomes

$$P_{DSE} = P_L \frac{R_F}{Z_0} \cdot \tag{11}$$

The reason for the four-fold increase in power absorbed for the shunt diode compared to the same series-mounted diode is the direct result of the line current doubling through the short circuit placed across the line by the shunt diode.

It is interesting to compare the product of power handling and insertion loss for the shunt and series diode, respectively,

$$P_{DSH} \times \alpha_{SH} = \left[\frac{4R_F}{Z_0} P_L\right] \frac{Z_0}{R_p} = 4P_L \frac{R_F}{R_p} \tag{12}$$

$$P_{DSE} \times \alpha_{SE} = \left[\frac{R_F}{Z_0} P_L\right] 4 \frac{Z_0}{R_p} = 4P_L \frac{R_F}{R_p} \cdot \tag{13}$$

This equivalency of shunt and series diode high-power performance insertion-loss product was pointed out by Muehe in an analysis of high-power gas duplexers.[8] His comparison also shows that the same relationship holds for the branched duplexer and the phase shift duplexer and is valid even when the gas tubes (or diodes) are decoupled by transformers or cavity techniques.

It is necessary to examine the bandwidth properties of shunt and series diode limiters in order to compare their capabilities. Two bandwidths of interest are: 1) the high-power isolation bandwidth, and 2) the receive (small signal) bandwidth.

The high-power isolation of the series mode limiter is determined by the reflected power during limiting. If the diode impedance is $Z = R_F + jX_L$, then the series mode isolation N is given by

$$N_{SE} = 10 \log \left[\frac{\left(\frac{R_F}{Z_0} + 2\right)^2 + \left(\frac{X_L}{Z_0}\right)^2}{\left(\frac{R_F}{Z_0}\right)^2 + \left(\frac{X_L}{Z_0}\right)^2}\right] \cdot \tag{14}$$

The shunt mode limiter high-power isolation is

$$N_{SH} = 10 \log \left[\frac{\left(\frac{1}{2} + \frac{R_F}{Z_0}\right)^2 + \left(\frac{X_L}{Z_0}\right)^2}{\left(\frac{R_F}{Z_0}\right)^2 + \left(\frac{X_L}{Z_0}\right)^2}\right] \cdot \tag{15}$$

A direct comparison of isolation for series and shunt modes can be made in the high-isolation approximation ($R_F \ll Z_0$ and $X_L \ll Z_0$)

$$N_{SE} \approx 10 \log \left[\frac{4}{\left(\frac{R_F}{Z_0}\right)^2 + \left(\frac{X_L}{Z_0}\right)^2}\right] \tag{16}$$

$$N_{SH} \approx 10 \log \left[\frac{\frac{1}{4}}{\left(\frac{R_F}{Z_0}\right)^2 + \left(\frac{X_L}{Z_0}\right)^2}\right] \cdot \tag{17}$$

It has been shown that, for equivalent line impedance, the isolation is 12 dB greater in the series mode. Since the isolation decreases 6 dB per octave in each mode, the series mode limiter also has a four-fold increase in isolation bandwidth over the shunt mode limiter. Graphic data for these two cases has been presented by Garver.[1]

The receive bandwidth is controlled by the loaded Q_L of the low-level limiter circuit. The Q_L of the shunt diode limiter of Fig. 2(b) is given by

$$Q_{LSH} = \frac{Z_0}{\left(2 + \frac{G}{Y_0}\right) \frac{1}{\omega_0 C_J}} \cdot \tag{18}$$

As the diode normalized conductance is generally less than 0.2 (1 dB loss) the shunt loaded Q_L becomes

$$Q_{LSH} \approx \frac{Z_0 \omega_0 C_J}{2} \cdot \tag{19}$$

In terms of normalized diode susceptance

$$Q_{LSH} \approx \frac{b_c}{2} \cdot \tag{20}$$

The Q_L of a series mounted diode is given by

$$Q_{LSE} \approx 2b_c. \tag{21}$$

Therefore the loaded Q_L of the shunt diode limiter is one-fourth that of the series diode circuit (for equivalent line impedance) and has four times the bandwidth.

Summarizing the comparison we have:

Shunt diode limiter

$$P_{DSH} = P_L \frac{4R_F}{Z_0}$$

$$\alpha_{SH} \approx \frac{Z_0}{R_p}$$

$$N_{SH} \approx 10 \log \left[\frac{\frac{1}{4}}{\left(\frac{R_F}{Z_0}\right)^2 + \left(\frac{X_L}{Z_0}\right)^2}\right]$$

$$Q_{LSH} \approx \frac{Z_0 \omega_0 C_J}{2}$$

Series diode limiter

$$P_{DSE} = P_L \frac{R_F}{Z_0}$$

$$\alpha_{SE} \approx 4 \frac{Z_0}{R_p}$$

$$N_{SE} \approx 10 \log \left[\frac{4}{\left(\frac{R_F}{Z_0}\right)^2 + \left(\frac{X_L}{Z_0}\right)^2} \right]$$

$$Q_{LSE} \approx 2Z_0\omega_0 C_J$$

In the preceding discussion, the choice of impedance level was arbitrary. Over the normal radar bandwidths (10 to 20 percent) broadband transformers can be used which in themselves do not effect the bandwidth. If the impedance is chosen such that

$$Z_{0SH} = 4Z_{0SE}$$

then

$$P_{DSH} = P_{DSE}$$

$$\alpha_{SH} = \alpha_{SE}$$

$$N_{SH} = N_{SE}$$

$$Q_{LSH} = Q_{LSE}.$$

Now the equivalence between the shunt and series circuits becomes apparent. However, there are other aspects to be considered.

The most common usage of a diode limiter allows the high power to be reflected back to the input. In this case, the simple shunt circuit of Fig. 1(a) has the following advantages:

1) The diodes are mounted from inner to outer conductors simplifying heat sinking and diode removal.
2) No circulator is required to direct the signal to the output as is required in Fig. 1(c).
3) Additional high-power isolation is easily obtained by adding a low-power limiting stage one-quarter wavelength behind the high-power input diode stage. Also, this has the effect of broadening the receive bandwidth. Alternatively, the second stage may be a low-power broadband limiter in itself; this would not effect the bandwidth but would enhance the high-power isolation.

In those cases where a nonreflective limiter is required in both high- and low-power states, the circuits of Fig. 1(b) through (f) may be used. In the circulator limiter circuit of Fig. 1(c), the high-power isolation is primarily controlled by the circulator (typically 25 dB) and is therefore not favorable for high-isolation requirements. A second disadvantage is the additional receive loss associated with the necessity of traversing the circulator twice. The balanced series limiter of Fig. 1(d) is also isolation limited, since it is basically controlled by the input hybrid isolation. To obtain higher values of isolation (60 to 80 dB are typical), it would be necessary to cascade two or more balanced arrays with a resulting increase in insertion loss, size, and complexity.

The balanced shunt limiter of Fig. 1(b) and the branched limiter of Fig. 1(e) are the preferred limiters for nonreflective applications. Either circuit can be used for duplexing applications by replacing a load with the antenna port. By adjusting line impedances, the high-power capability of each diode stage, the insertion loss, and the high-power isolation can be equalized. The choice between the two circuits is generally dictated by size and the receive bandwidth. By using three-quarter wavelength 3 dB hybrids, it is possible to obtain double-octave bandwidth with the balanced limiter approach. The bandwidth of the branched limiter is somewhat limited by the necessity of using a quarter wavelength spacing between the T junction and the shunt diode. An alternate branched limiter is shown in Fig. 1(f), with the series diode replaced by a shunt diode located at the end of a quarter wavelength stub. This improves the high-power bandwidths at the expense of further degrading the receive bandwidth. For 10 percent nominal bandwidths, both the balanced and the branched limiters are comparable in performance.

In order to enhance power handling, it is possible to parallel N diodes to obtain current sharing with a resulting power handling increase given by

$$P_{LSH} = P_D \frac{N^2 Z_0}{4R_F} \cdot \tag{22}$$

$$P_{LSE} = P_D \frac{N^2 Z_0}{R_F} \cdot \tag{23}$$

Thus, power handling varies directly with the power dissipation capability of the diode, line impedance, and the square of the number of diodes used.

The insertion loss resulting from the use of multiple diodes becomes

$$\alpha_{SH} = N \frac{Z_0}{R_p} \cdot \tag{24}$$

$$\alpha_{SE} = 4N \frac{Z_0}{R_p} \cdot \tag{25}$$

The loaded Q_L of a multiple diode stage becomes

$$Q_{LSH} \approx N \frac{Z_0\omega_0 C_J}{2} \tag{26}$$

$$Q_{LSE} \approx N2Z_0\omega_0 C_J. \tag{27}$$

The isolation resulting from the use of multiple diodes increases by a factor of N^2.

Solving (22) and (24) simultaneously (eliminating Z_0 as a variable) yields the obtainable power handling capability in terms of the diode parameters and the allowable insertion loss

$$P_{LSH} = \frac{NP_D R_p \alpha}{4R_F} \cdot \tag{28}$$

For a given diode, P_D, R_p, and R_F are constants. For a given insertion loss, the ability to handle large amounts of power is proportional to the number of diodes used. This

expression is valid for both the shunt and series modes of operation. It is also valid for series stacked diodes, although this technique is not normally used due to increased complexity associated with heat sinking the individual diodes.

Alternatively (22) and (26) may be solved simultaneously yielding power handling capability in terms of the diode parameters and the allowable loaded Q_L

$$P_{L_{SH}} = \frac{NP_DQ_{L_{SH}}}{2R_F\omega_0C_j} . \tag{29}$$

For a given number of diodes, loaded Q_L, diode R_F, and C_J, it is apparent that it is advantageous to maximize P_D. This suggests the use of a thick diode which has a larger volume and greater power handling capability for a given capacitance than does a thin diode. The limitations of the thick diode are the effects it may have on R_F and some parameters not shown in (29). Conceptionally at least, R_F may be held constant by increasing the diode height and area at the same rate. This may be visualized as series stacking N diodes while at the same time, paralleling N stacks, thus preserving C_J, R_F, and R_p. The power handling capability of this new $N\times N$ diode is increased by N^2. This, of course, is a simplified model, since effects such as turn-on time, current sharing, and thermal resistance have not been considered.

The constraint placed on upper junction thickness for limiter diodes can result in 1) the appearance of spike leakage, 2) higher power absorbed within the junction, and 3) increased insertion loss. The first two problems are solved in switched limiters and duplexers by forward biasing the diodes into a low R_F state during the transmit state, and the last problem is aided by reverse biasing the diode to increase R_p during the receive state. Since this paper discusses only passive limiters and duplexers biasing is not allowable. A subsequent section will analyze the advantages and disadvantages of thick diodes in more detail.

In order to build a multiple diode limiter (or passive diode duplexer) to handle a required line power P_L a number of decisions have to be made. The first choice is generally the type of diode required. In order to minimize the number of diodes to be used in the high-power stage (N diodes assumed in parallel), P_D is maximized for a given C_J consistent with constraints previously discussed. Once a diode is chosen with a given P_D, C_J, R_P, and R_F, it can be paralleled to N diodes in order to satisfy the line power commitments. The constraint upon N (not considering the mechanical design problem) is whether the insertion loss or loaded Q_L is violated. Generally the high-power isolation is not a prime consideration (in the shunt limiter) as this may be solved by subsequent low-power (lowloss) clean-up stages. As previously explained, the series mode limiter is not normally used in high-isolation requirements as high-power stages have to be cascaded to increase the high-power isolation. Solving (1), (24), and (26) simultaneously results in an insertion loss, loaded Q_L, diode Q_D criteria

$$Q_D' = 2\frac{Q_L}{\alpha} . \tag{30}$$

This equation yields a unique value of diode Q which results in a limiter meeting the loaded Q requirement and the insertion loss simultaneously. The use of a single stage of N diodes tuned to parallel resonance is assumed. If a higher diode Q is available the loaded Q_L becomes more critical than the insertion loss, and conversely, a lower diode Q will result in the insertion becoming more critical than the loaded Q. Four generally encountered cases will now be discussed.

For those applications where it is advantageous to use a single stage of diodes shunt mounted in a 50 ohm coaxial line impedance (eliminating the need for transformers), (28) is solved for N diodes of a suitable type to handle the required power P_L with an allowable insertion loss α. This results in a loaded Q as in (26) which may or may not be satisfactory. Alternatively, (29) can be solved for a given Q_L yielding the minimum number of diodes required. The resulting insertion loss is then determined.

A more versatile design is one in which the line impedance may be varied, by transformation techniques, to take advantage of the trade-offs allowed by the circuit theory. If a diode Q is available which exceeds Q_D', the minimum number of diodes necessary to handle the line power P_L is given by (29) for the loaded Q desired. The required line impedance is calculated from (26). It should be noted that the resulting insertion loss is lower than the required insertion loss by the ratio of the actual diode Q to Q_D'.

For those cases where a diode is used with a Q less than Q_D', (28) should be solved for N using the allowable insertion loss. The required line impedance is calculated from (24) and the resulting loaded Q calculated from (26). Here, Q_L will be lower than that required by the ratio of the diode Q to Q_D'.

In the special case where Q_D equals Q_D', the insertion loss and the loaded Q_L will approach the specified limits simultaneously as either N or Z_0 is varied. For a conventional radar bandwidth of 10 percent, a loaded Q_L of the order of 1.5 is normally required if a single stage (parallel tuned to resonance) diode limiter is used. Assuming an allowable insertion loss of 0.5 dB, α_{SH} is approximately 0.1 resulting in a diode Q of 30 from (30). For limiter applications, diodes are available with a cutoff frequency of the order of 150 GHz. This would mean that single stage limiters constructed below 5 GHz would be bandwidth (Q_L) restricted whereas above 5 GHz, the limitation would be insertion loss. This analysis is a restricted one as it does not include the effects of parasitic inductance or capacitance which generally becomes important above 1 GHz.

Choice of Diode Type

It was shown in (22) that for a given line impedance and number of diodes, the maximum line power is directly proportional to the ability of the diode to absorb power (P_D), and is inversely proportional to the diode forward conduction resistance (R_F). Both of these conditions dictate the use of a large diode. There are two important constraints placed upon diode size: 1) a maximum allowable capacitance is determined by either insertion loss or bandwidth, or both;

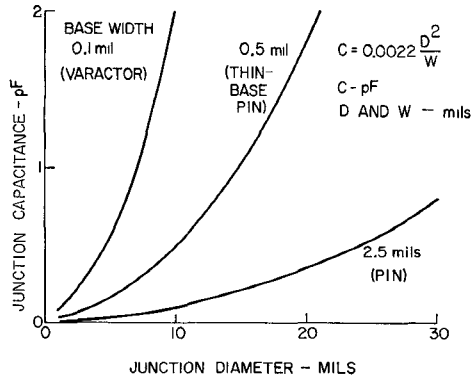
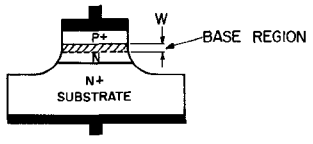


Fig 3. Calculated junction capacitance versus junction diameter.



	VARACTOR	THIN-BASE PIN	PIN
W (mils)	0.1	0.5	2.5
DIA. (mils)	1-4	5-10	20-50
VOLTAGE	40	200	800
RESISTANCE(Ω)	0.7	0.7	0.7
THETA °C/ω	150	40	15

Fig. 4. Typical junction diode types.

and 2) the thickness W of the diode is determined by the rectification efficiency of the diode at the desired operating frequency.

Considering the small signal equivalent circuit of the diode as essentially a parallel plate capacitor with a dielectric constant of 12 (for silicon), a capacity of 0.002 pF per circular mil is obtained for a 1 mil junction thickness W. The junction size for conventionally available varactor and *PIN* diodes is shown in Fig. 3. The considerable increase in size is made possible with a thick I-region *PIN* diode, compared to the smaller depletion layer associated with a varactor diode. If, for example, an 0.8 pF maximum junction capacity is allowed, the resulting junction diameter would be 6 mils for the varactor and 30 mils for the *PIN* diode. The increase in area for the *PIN* diode is 25 to 1, and the increase in volume is 625 to 1 compared to the varactor diode.

Fig. 4 shows typical diode parameters for a conventional limiter type varactor diode, a thin-base *PIN*, and a switching type high-voltage *PIN* diode. The breakdown voltages are of interest as a rough measure of the junction thickness. In a limiter or passive duplexer application, the diode conducts under high power, and therefore only RF current need be considered. In the passing state the diode sustains the line voltage, but this is the small signal receive state, and the voltage associated with it is necessarily below the diode limiting level which is approximately 1 volt. The diode breakdown voltage is not, therefore, a direct determining factor in power handling.

The heat transfer characteristic of the junction is determined by the diode theta given in degrees per watt dissipated. Since this is a steady-state parameter, it is a direct measure of CW power handling capabilities of the junction for a maximum allowable temperature rise. The transient temperature response to a dissipative pulse has been theoretically studied by Mortenson[9] who has indicated an initial linear temperature rise followed by a square root of time dependence.

For narrow-pulse operation, the ability of a junction diode to handle pulsed microwave power can be calculated on a heat capacity basis that assumes no junction cooling—a conservative calculation useful for gaining insight into the approximate power handling capability of a given junction size. The heat capacity H is given in watt-microseconds by

$$H = \text{volume} \times \text{density} \times \text{specific heat} \tag{31}$$

$$H = 0.025\ D^2W \text{ watt-microseconds/°C} \tag{32}$$

where D is the junction diameter in mils, and W is the junction thickness in mils.

From (32) the heat capacity is directly proportional to the junction volume. The junction capacitance is given by

$$C_J = \epsilon(8.85 \times 10^{-12}) \frac{A}{W} \text{ farads/meter} \tag{33}$$

where ϵ is the dielectric constant (12 for silicon), A is the junction area in square meters, and W is the I-region thickness in meters.

For a silicon dielectric, converting into picofarads and mils, the junction capacitance becomes

$$C_J = 0.0022 \frac{A}{W} \text{ picofarads} \tag{34}$$

where A is expressed in square mils and W is expressed in mils. This equation is plotted in Fig. (3). By substituting (34) into (32), the heat capacity is given in terms of the junction thickness

$$H = 11 C_J W^2 \text{ watt-microseconds/°C} \tag{35}$$

where C_J is in picofarads and W in mils.

Equation (35) indicates that for a maximum allowable capacity C_J, the heat capacity is proportional to the junction thickness W squared, illustrating the need for thick junctions for maximum power handling.

There is, however, a constraint placed upon junction thickness. This is the ability of the junction to rectify quickly and efficiently at microwave power levels. If the diode fails to rectify, a number of undesirable effects are produced. Slow response of the diode, in relation to the frequency, may allow a large spike of power to pass before appreciable limiting is achieved. Coincident with this is the fact that the diode is passing from a high-impedance to a low-impedance state as a function of time. The absorbed power can increase to a maximum of 50 percent of the applied power as the conductances pass through a normalized value of 2. Thus, considerable amounts of power can be absorbed during the diode conduction time, and it is obviously an advantage to have the diode pass through this state quickly.

Another problem is the zero bias "punch-through" effect, which is the ability of the junction to reach its mini-

mum capacitance at zero applied dc voltage. If this punch-through is not achieved, insertion loss will be excessive. Punch-through occurs when the depletion layer extends across the entire *I* region. If this does not occur, the unswept region of the diode acts as a lossy capacitor, considerably raising the insertion loss. The punch-through diode becomes more difficult to achieve as junction thickness increases. Typically, a 1 mil thick *I* region (25 microns) is the maximum zero-bias punch-through junction obtained using 5000 Ω/cm silicon. To achieve punch-through for a 3 mil *I*-region junction, greater than 15 000 Ω/cm silicon would have to be used, a value considered beyond today's state of the art.

An experimental determination was made of the maximum junction thickness as a function of maximum operating frequency. The criterion for successful operation was the selection of the maximum frequency at which a barely observable spike was obtained on an oscilloscope. From experience it was known that during the onset of this spike leakage, the power absorbed within the diode was excessive and the power handling considered marginal. No quantitative data was taken on power absorbed, therefore the experimental data on spike leakage is offered only as typical behavior for the particular diodes used. It is known that the spike amplitude is also a function of pulse risetime and carrier lifetime in the junction. To perform the test, the diodes under observation were shunt mounted across a 50 ohm coaxial line. The pulsewidth was 1 μs with a risetime of the order of 50 ns. The power was applied at a low level and then slowly increased until limiting took place. If the frequency is low enough the diode output response will pass smoothly through the limiting threshold into a nearly constant power output region. As the frequency is increased, a point is reached where a spike is formed as the diode output passes through the limiting threshold, followed during the rest of pulse, by a reasonably constant flat leakage. This is a familiar effect seen with gas T–R tubes and ferrite limiters. The data shown in Fig. 5 are given for four junction thicknesses: 0.1, 0.5, 1.0, and 1.4 mils. In the range from 50 to 150 MHz it is possible to use a junction thickness of approximately 1.0 mil. For frequencies between 500 and 900 MHz, the thickness must be restricted to the order of 0.5 mil. Varactor diodes with a depletion region of 0.1 mil, or less, are commonly used at *X* band and above. It should be recognized that the data shown in Fig. 5 are unique to the particular diodes used and will vary as the diode lifetime or pulse risetime is changed. Nevertheless, the data does illustrate, even if only qualitatively, a constraint imposed upon the maximum allowable junction thickness when these diodes are used in a passive limiter application.

The relationship of power handling to junction thickness is demonstrated in Fig. 6 for the varactor, the thin-base *PIN*, and the *PIN* diodes. The criterion for maximum power absorption is a maximum allowable junction temperature rise of 75°C. This was measured in two ways, one technique for the *PIN* and another for the varactor. Due to the slow response of the *PIN* diode at 300 MHz, it was necessary to dc forward bias the junction to prevent burnout. To estimate temperature rise in the forward biased junction during microwave pulsed power, the diode was previously calibrated as a thermometer. This was done by measuring the forward voltage drop as a function of ambient temperature while constant bias current was applied. By observing the pulse voltage change on an oscilloscope, an estimate was made of the peak temperature rise obtained.

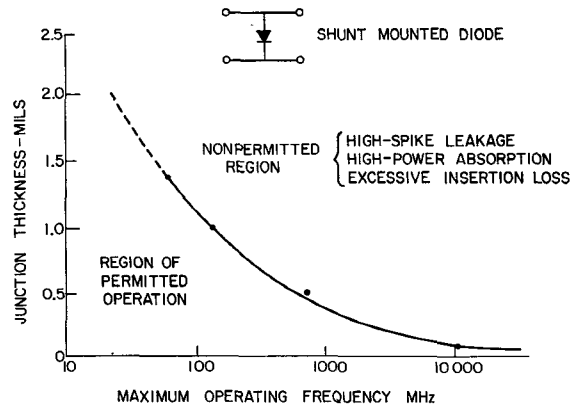


Fig. 5. Junction thickness versus maximum operating frequency.

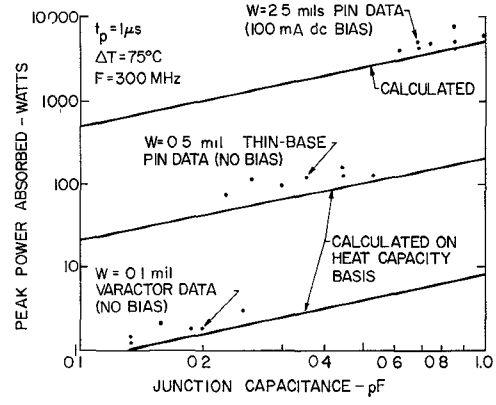


Fig. 6. Peak power absorbed versus junction capacitance.

Since it was not desirable to bias the varactor and the thin-base *PIN* diodes, in order to operate them as self limiters, an alternate technique of temperature monitoring was used. By injecting a low-level probing signal into the RF line during the interpulse interval, it was possible to measure diode recovery time as a function of power and pulsewidth. Recovery time is defined as that time necessary for the diode to return from its blocking state to within 3 dB of its receiving state. This is a common measurement used in T–R tubes. A plot of the data taken (Fig. 7) indicates that the diode recovery time is proportional to peak power and pulsewidth. The point A, where nonlinearity of the curves begins, is considered as the onset of excessive junction heating. Point B is considered as a point of catastrophic failure due to a runaway temperature condition. From experience, we know that point A corresponds to a 75°C temperature rise and, therefore, can be successfully used as a measuring point for diode power handling without danger of subsequent diode failure.

Using these two techniques the power handling capability of the three diode types was obtained and is plotted in Fig. 6. It is evident that for a given diode type, power handling in-

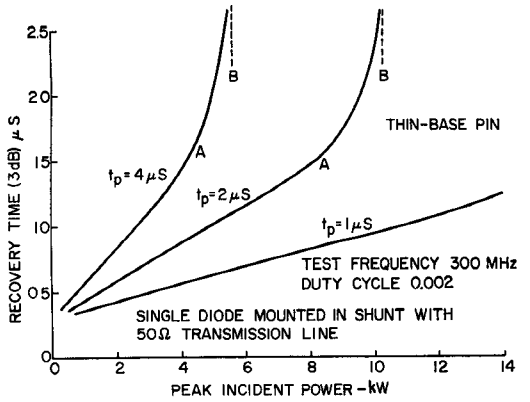


Fig. 7. Recovery time versus peak power.

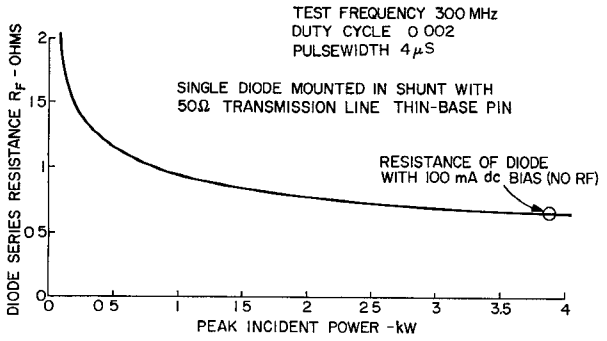


Fig. 8. Diode series resistance versus peak power.

creases with junction capacitance. More importantly, a substantial improvement in power handling is achieved by using significantly thicker diode junctions. The 2.5 mil *PIN* diode demonstrates an ability to absorb 5 kW of 1 μs RF power when forward biased with 100 mA dc. Unfortunately this diode cannot be successfully used as a passive limiter because of its slow response in the VHF range. It is possible to overcome this problem by placing a crystal diode preceding the *PIN* diode to sample a small portion of the applied RF power, rectifying it, and feeding it to the *PIN* to drive it into conduction. This technique, although used successfully for single diode stages, is considered too complex in multiple diode applications.

The power handling capability of the 0.5 mil thin-base *PIN* shown in Fig. 6 is approximately 25 times greater than the equivalent capacitance varactor, consistent with (35), and adequately demonstrates the advantage of using a thick-junction diode for power handling enhancement at UHF frequencies. It was not possible to use 1.0 mil junctions at UHF frequencies due to excessive insertion loss resulting from a lack of punch-through effect.

A plot of the thin-base *PIN* series resistance versus peak power is shown in Fig. 8. The measurement was performed at 300 MHz with a 4 μs applied pulsewidth. The reduction of R_F with increasing peak power indicates that the electron-hole density within the *I* region is still increasing as a function of RF current. This effect is similar to that experienced with the gaseous plasma of T–R tubes. In the RF current state (4.0 kW line power represents 18 ampere short-circuit current) the resistance of the diode junction approaches the forward bias resistance, 0.7 ohms, with 100 mA dc bias current. To achieve the same level of diode resistance that results with a 100 mA dc bias, the equivalent RF current must be 18 amperes, a difference in effectiveness of 45 dB. Similar results of even larger magnitude have been reported at *X* band.[10]

High-Power Limiter Design

The choice of diode type has been based on the largest possible junction thickness consistent with acceptable self-limiting properties in the VHF and UHF bands. Once a diode has been selected, power handling capability can be increased in proportion to the square of the number of diodes mounted in parallel. A high-power limiter mount was designed incorporating 31 thin-base *PIN* diodes inserted in radial fashion around the perimeter of a $3\frac{1}{8}$ inch coaxial transition.[11] This transition, shown in Fig. 9, is actually a quick step transition to a type *N* output line. The capacitance of the diodes is parallel resonated to a low VSWR, less than 1.10, by inserting an inductance across the transmission line. A boron nitride dielectric spacer was used to align the center conductor to the outer conductor, and offer a heat sink path to the outer conductor. The diodes can be easily replaced by removing a single threaded bushing containing the diode. This limiter is shown in Fig. 10.

The insertion loss and bandwidth of the 55 MHz limiter are depicted in Fig. 11 by the dashed lines. A minimum loss of 1 dB was obtained with a 3 dB bandwidth of 90 MHz. By varying the tuning inductance the limiter could be tuned from 30 to 450 MHz. Insertion loss increases with frequency as shown by the solid curve in the figure. For a completely punched-through diode limiter, the insertion loss would be expected to increase as the square of the frequency. The slower increase in loss with frequency obtained for this limiter indicates that complete punch-through was not achieved. The diodes appeared as a lossy capacitor deteriorating the diode *Q* at the low frequencies, resulting in higher loss than expected.

The high-power performance of the thin-base *PIN* diode limiter was tested by utilizing cavity power multiplication techniques up to 1 MW peak, 1500 watts average power, with a 4 μs pulsewidth.

Based on individual diode tests, a capability of handling over 10 mW peak power can be calculated for the 31 diode limiter. If necessary, it is possible to further enhance power handling capability by taking advantage of a favorable trade-off between the line impedance Z_0 and the number of diodes *N*. By maintaining the product (NZ_0) constant, in a single diode stage, it is possible to increase power handling capability proportional to the number of diodes used. The compromise one must pay is the necessity of using matching transformers to obtain lower values of line impedance (in order to increase *N*) thus increasing the size of the limiter.

In the 55 MHz limiter, previously discussed, the bandwidth was obtained by a parallel resonant circuit technique. The loaded Q_L of *N* diodes in such a circuit has been shown

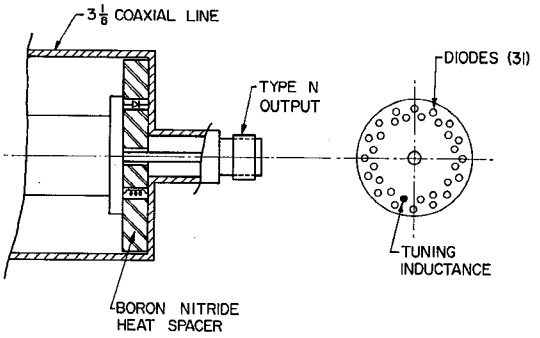


Fig. 9. VHF limiter configuration.

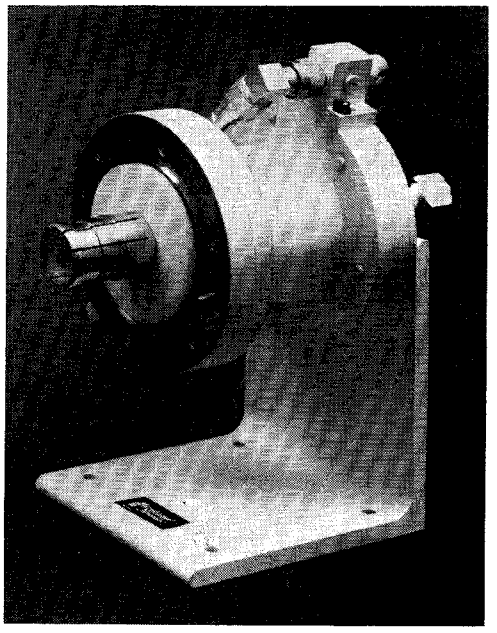


Fig. 10. VHF high-power limiter.

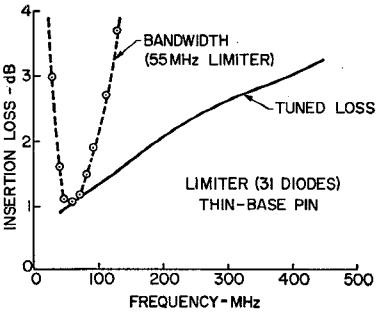


Fig. 11. Receive loss versus frequency.

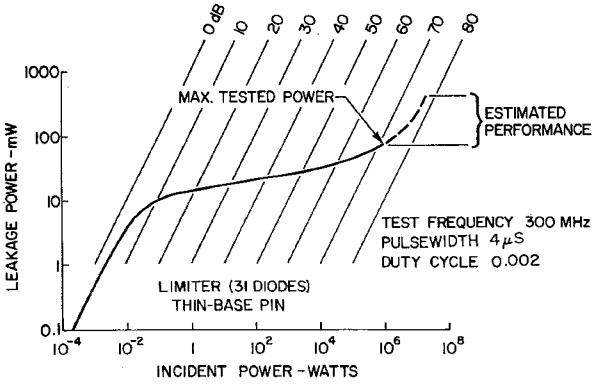


Fig. 12. Leakage power versus incident power.

to be proportional to NZ_0 [see (26)]. The loaded Q_L is therefore not changed if NZ_0 is maintained constant. The ability to broadband the diode tuned circuit beyond its inherent bandwidth is then controlled by the transformer design. It is well known that for a given element Q_L greater bandwidth is obtained by increasing the number of external tuning elements. The maximum bandwidth obtainable is given in a theorem by Bode[13] who establishes the maximum reflection loss realizable in a given band in the presence of parasitic shunt reactance. These results can be written as

$$\ln \left|\frac{1}{\Gamma}\right| \leq \frac{\pi}{\Delta\omega R C_J} \tag{36}$$

where

Γ is the voltage reflection coefficient
C_J is the junction capacitance
R is the load and losses
$\Delta\omega$ is the bandwidth of interest.

In general, most radar duplexing and receiver protection bandwidths are in the order of 10 percent and extended bandwidth techniques are not required.

The receiver protection capabilities of the high-power limiter is shown in Fig. 12. The test frequency was 300 MHz with a pulsewidth of 4 μs. The threshold of limiting occurred at approximately 10 mW peak power with an essentially constant output power of 10 to 50 mW peak power obtained over nearly an 80 dB dynamic range. Above 1 MW, the limiter approached a maximum isolation of 80 dB. This maximum isolation consisted of the high-power limiter stage isolation of 60 dB, followed by a second low-power low-loss varactor stage of 20 dB isolation. Due to a diode response time on the order of 10 ns, compared to an RF risetime of 50 ns, the spike leakage energy was negligible. Based on individual diode tests, a capability was demonstrated for handling over 10 MW peak power with a 1 μs pulsewidth.

High-Power Diode Duplexer

A high-power all-diode duplexer was built and successfully tested at 200 MHz under extremely wide pulsewidth conditions.[13] This duplexer, shown in Fig. 13, consisted of a high-power input hybrid of the 3⅛ inch coax reverse-wave type, with a low-power stripline hybrid in the output. The two colinear output ports of the input hybrid were terminated with radial-diode type high-power limiters. Each limiter section consisted of sixteen 1 mil thick I-region thin-

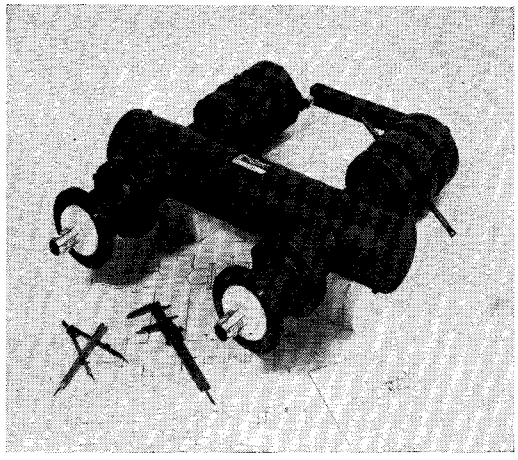


Fig. 13. 200 MHz diode duplexer.

base *PIN* diodes of 2 pF junction capacitance each. As these diodes are essentially five times larger in area than the previously described thin-base *PIN*, an excellent high-power capability was achieved. This duplexer was tested in an operational radar installation at 150 kW peak power, 10 kW average power, with a pulsewidth of 200 μs. A maximum transmit loss of 0.15 dB was obtained under high-power conditions with no cooling of any kind. The receive loss was 2 dB over the operating bandwidth of 200 to 225 MHz. An experiment was performed to check for diode punch-through. By reverse biasing all 32 diodes with 1 volt dc, it was found that the insertion loss could be reduced to 1.0 dB. This test confirmed that the diodes were not fully punched through. This device could also be used as a reflectionless limiter as shown in Fig. 1(b).

The high-power thermal effects within the diode junction are considerably different in this long pulse application compared to the narrow-pulse (4 μs) operation discussed for the high-power limiter design. As the 200 μs pulsewidth is longer than the thermal time constant of the diodes used (about 150 μs), the pulse heating is approaching its steady-state (CW) value. This means that it is necessary to use diodes with a low CW thermal resistance generally associated with large area junction. In order to minimize the capacity per unit area, diodes are again used with a thickness consistent with the speed of allowable response. As considerable diode cooling takes place during the long pulse operation, it is advantageous to heat sink the diode as efficiently as possible, a consideration of lesser importance in narrow-pulse low-duty cycle applications.

The peak junction temperature T_J is determined by the heat sink temperature T_S, the diode peak temperature rise ΔT_P, and the diode average temperature rise ΔT_A. A simplified expression can be used for the total junction temperature by assuming that peak heating commences at the average temperature rise. In actuality, the average temperature rise lies between the minimum and maximum of the repeated transients caused by the pulsed power.

$$T_J = T_S + \Delta T_P + \Delta T_A \tag{37}$$

$$T_J = T_S + P_{DP}\theta_P + P_{DA}\theta_A \tag{38}$$

where

P_{D_P} is the peak pulsed power dissipated within the junction
θ_P is the thermal resistance, a function of pulse length
P_{D_A} is the average power dissipated within the junction
θ_A is the steady state (CW) thermal resistance.

In wide-pulse medium-duty-cycle applications (such as the 200 μs pulsewidth, 6 percent duty cycle previously described) the peak heating effect dominates, since the third term of (38) can be neglected. In other applications with narrower pulsewidths and higher duty cycles, the effects of average power heating may dominate. Generally, a peak junction temperature on the order of 100°C is considered acceptable.

Conclusions

A theoretical comparison of the series and shunt mode of diode mounting reveals that equivalent performance is obtained for receive loss, power handling, bandwidth, and high-power isolation by adjusting the line impedance. In practice, the series mode limiter is not advantageous because of the difficulty in obtaining large values of high-power isolation. The method of cascading a low-power diode stage behind the high-power shunt diode stage is very practical, and is similar to the well-known gas T–R tube concept of multiple discharge stages.

Both theoretical calculations and experimental data show the merits of using a thick junction diode for high-power handling capability. Diode thickness, however, is constrained by the possible operating frequency range. Thick diode junctions have slow response and consequently at some upper frequency, the diode is incapable of efficient rectification, resulting in high spike leakage and excessive dissipated power. The thin-base *PIN* diode is the largest diode known capable of passive limiting in the VHF and UHF frequency range. To minimize the receive loss, a zero-bias punch-through diode is required. For thick diodes, high-resistivity silicon is required to achieve this punch-through.

High power performance of the thin-base *PIN* diode limiter has a number of characteristics similar to those observed in gas T–R tubes. The recovery time of the diode is a function of power and pulsewidth. The diode conductive resistance decreases as the applied power is increased. Both of these effects are known to occur in gas T–R tubes.

The thin-base *PIN* diode can be designed into practical high-power limiters and duplexers. The advantages of these all-diode devices compared to gas devices is their speed of response, absence of required control voltage (keep-alive), and a potential for long-life operation free of increasing loss and recovery time.

ACKNOWLEDGMENT

The author would like to thank P. Basken, D. Conlon, A. Wonson, and H. Griffin of Microwave Associates, Inc. for their contributions to this paper. The author is also indebted to Dr. K. E. Mortenson of Rensselaer Polytechnic Institute, Troy, N. Y., for his encouragement, suggestions, and faith in the validity of the thin-base *PIN* concept.

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Frequency Modulation of Avalanche Transit Time Oscillators

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Abstract—**This paper presents experimental data taken to determine the frequency modulation characteristics of avalanche transit time oscillators.**

The active element is a diffused mesa diode with a shallow junction in epitaxial *n*-*n*+ silicon; the details of the construction of the diode are presented and its typical characteristics are discussed.

The basic oscillator consists of the diode mounted in the capacitive portion of a radial mode cavity machined of copper with the outlines of a DO-5 diode header. The frequency of oscillation is dependent upon the diode junction capacitance and is varied between 5 and 8 GHz for the diodes tested. Microwave power levels up to 100 mW have been observed with an efficiency exceeding 3 percent. The frequency drift over the temperature range from −70 to +100°C is 2.5×10^{-5} parts/°C.

The frequency modulation characteristics of these oscillators indicate their potential applications in miniature solid-state low-power communications systems.

ELECTRONIC tuning of avalanche transit time oscillators has been treated explicitly by Gilden and Hines.[1] This electronic tuning effect, which is attributed to the variability of avalanche susceptance with current, is evident also in theoretical and experimental investigations of others for both Read and *p*-*n* type devices.[2],[3] Read[4] has discussed electronic tuning briefly but was uncertain as to whether the variation of frequency of oscillation with the diode current could be made large enough for a practical frequency-modulation device, particularly when the diode was operating at optimum frequency and bias. For transit angles substantially less than the optimum value, however, Gilden and Hines showed that strong negative resistance effects still occurred and that electronic tuning effects were significant. Recently, Rulison *et al.*[6] reported a germanium *p*-*n* diode which exhibited a susceptance variation with current between a half and one order of magnitude larger than that of a Read diode under similar operating conditions.

Since moderate CW output power from these devices is now being realized, the ease of electronic tuning suggests their potential usefulness in many practical applications. This paper presents experimental data which were taken to determine the frequency modulation characteristics of avalanche transit time oscillators made at Sperry Microwave Electronics Company in terms of modulation linearity and inherent amplitude modulation.

The active element is a diffused silicon mesa diode, similar to the one described by Misawa.[5] The junction is formed by diffusing boron 2.4 microns deep in epitaxial silicon. The substrate is arsenic doped to a resistivity of 0.008 ohm/cm

Manuscript received May 17, 1967; revised September 30, 1967.

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